Main Function and Parameter:

- 500V,2A(Peak),1.2A(Continuous)
- Low-Side MOSFET open-source output

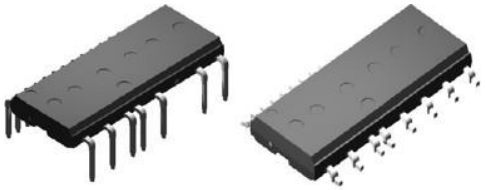
Features:

- Active-High interface, works with 3.3V/5V MCU；
- Built-In protection of Shoot through；
- HVIC for Under-voltage Protection；
- HVIC for Under-voltage Protection；
- Isolation Rating：1500V

Application:

- Air Fan
- Electric Power Tools

Package



DIP23-FP SOP23-FP

Order codes	Package	Marking
XP02M50AS0-C	DIP23-FP	XP02M50AS0-CD
	SOP23-FP	XP02M50AS0-CK

Internal Block Diagram

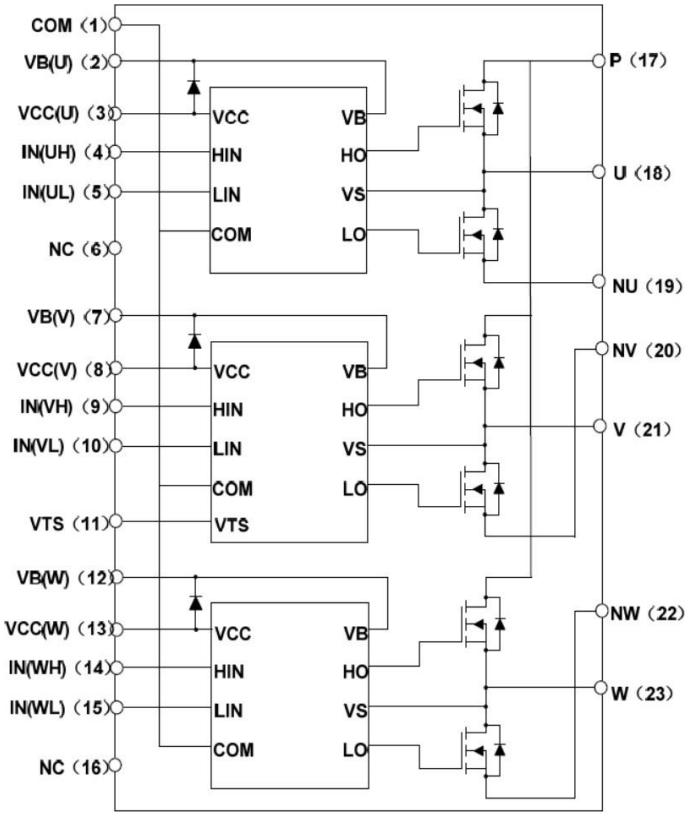


Fig 1： Internal Block Diagram

Pin Configuration

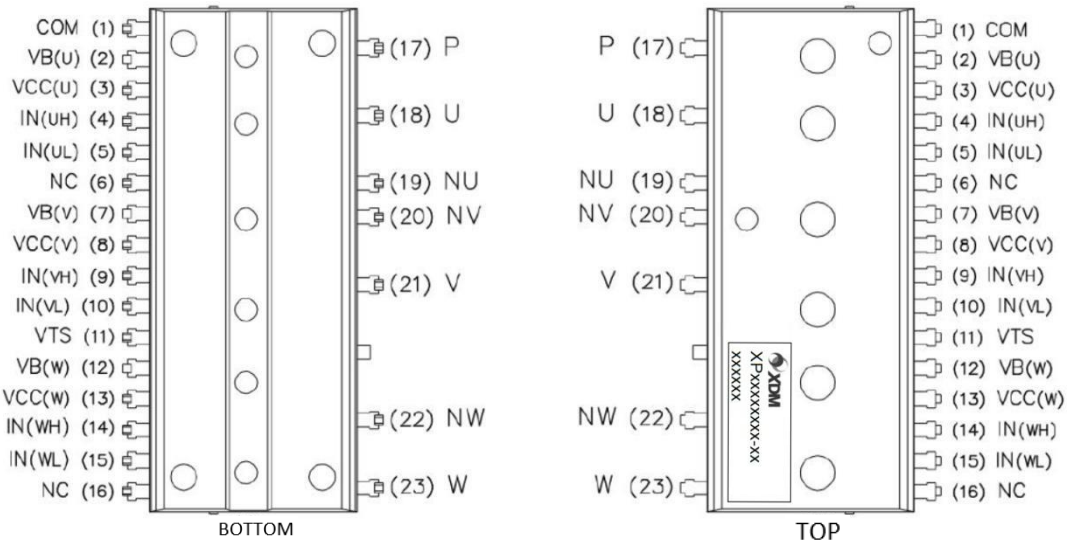


Fig 2 Pin Configuration

Pin Number	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	VB(U)	Bias Voltage for U-Phase High-Side MOSFET Driving
3	VCC(U)	Bias Voltage for U-Phase IC and Low-Side MOSFET Driving
4	IN(UH)	Signal Input for U-Phase High-Side
5	IN(UL)	Signal Input for U-Phase Low-Side
6	NC	No Connection
7	VB(V)	Bias Voltage for V-Phase High Side MOSFET Driving
8	VCC(V)	Bias Voltage for V-Phase IC and Low Side MOSFET Driving
9	IN(VH)	Signal Input for V-Phase High-Side
10	IN(VL)	Signal Input for V-Phase Low-Side
11	VTS	Output for HVIC Temperature Sensing
12	VB(W)	Bias Voltage for W-Phase High-Side MOSFET Driving
13	VCC(W)	Bias Voltage for W-Phase IC and Low-Side MOSFET Driving
14	IN(WH)	Signal Input for W-Phase High-Side
15	IN(WL)	Signal Input for W-Phase Low-Side
16	NC	No Connection
17	P	Positive DC-Link Input
18	U	Output for U-Phase & Bias Voltage Ground for High-Side MOSFET Driving
19	NU	Negative DC-Link Input for U-Phase
20	NV	Negative DC-Link Input for V-Phase
21	V	Output for V-Phase & Bias Voltage Ground for High-Side MOSFET Driving
22	NW	Negative DC-Link Input for W-Phase
23	W	Output for W Phase & Bias Voltage Ground for High-Side MOSFET Driving

Absolute Maximum Ratings (Tj= 25°C, Unless Otherwise Specified)

Inverter Part

Symbol	Parameter	Condition	Ratings	Units
V_{DSS}	Drain-Source Voltage of Each MOSFET		500	V
I_D	Each MOSFET Current, Continuous	Tc = 25°C (Tc refer to Fig:5)	1.2	A
I_{DM}	Each MOSFET Pulse Current, Peak	Tc = 25°C, less than 100us	2	A
I_{Drms}	Each MOSFET Current, Rms	Tc = 25°C, F_{PWM} <20KHz	0.85	Arms
P_D	Maximum Power Dissipation	Tc = 25°C , For Each MOSFET	14.2	W

Control Part

Symbol	Parameter	Condition	Ratings	Units
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied between VB and VS	20	V
V_{IN}	Input Signal Voltage	Applied between V_{IN} and COM	-0.3~V_{CC}+0.3	V

Bootstrap Diode Part

Symbol	Parameter	Condition	Ratings	Units
V_{RRMB}	Control Supply Voltage		500	V
I_{FB}	High-side Bias Voltage	Tc = 25°C	1	A
I_{FPB}	Input Signal Voltage	Tc = 25°C, Less than 1mS	2.5	A

Total System

Symbol	Parameter	Condition	Ratings	Units
Tj	Operating Junction Temperature		-40~150	℃
T_{STG}	Storage Temperature	Tc = 25°C	-40~125	℃
V_{ISO}	Isolation Voltage	60Hz, Sinusoidal, AC 1 min, between pins and heat-sink plate	1500	V

NOTE1: To insure safe operation of the IPM, the average junction temperature should be limited to TJ ≤ 150°C (@Tc ≤ 100°C).

Thermal Resistance

Symbol	Parameter	Condition	Ratings	Units
Rth(j-c)	Junction to Case Thermal resistance	For Each MOSFET	8.8	°C/W

Electrical Characteristics (TJ= 25°C, Unless Otherwise Specified)

Inverter Part

Symbol	Parameter	Condition	Min	Typ	Max	Unit
BV_{DSS}	Drain – Source Breakdown Voltage	V_{IN} = 0 V, I_D = 1 mA（Note2）	500	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{IN} = 0 V, V_{DS} = 500 V	-	-	1	mA
V_{SD}	Drain - Source Diode Forward Voltage	V_{CC} = V_{BS} = 15V, V_{IN} = 0 V, I_D =-0.5 A	-	0.8	-	V
$R_{DS(on)}$	Drain-Source Turn-On Resistance	V_{CC} = V_{BS} = 15 V, V_{IN} = 5 V, I_D =0.5 A	-	2.5	3.3	ohm
t_{ON}	Switching Times	V_{PN} = 300 V, V_{CC} = V_{BS} = 15 V, I_D = 0.5 A, V_{IN} = 0/5 V, Inductive L = 3 mH （Note3）	-	800	-	nS
t_{OFF}			-	450	-	nS
t_{rr}			-	200	-	nS
E_{ON}			-	38	-	uJ
E_{OFF}			-	8	-	uJ
R_{BSOA}	Reverse Bias Safe Operating Area	V_{PN} = 400 V, V_{CC} = V_{BS} = 15 V, I_D = I_{DP},V_{DS} = BV_{DSS},T = 150°C	Full square			

NOTE 2： BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each FRFET inside SPM®. VPN should be sufficiently less than this value considering the effect of the stray inductance so that VDS should not exceed BVDSS in any case.

NOTE 3: t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applcations due to the effect of different printed circuit boards and wirings. Please see Fig 3 for the switching time definition.

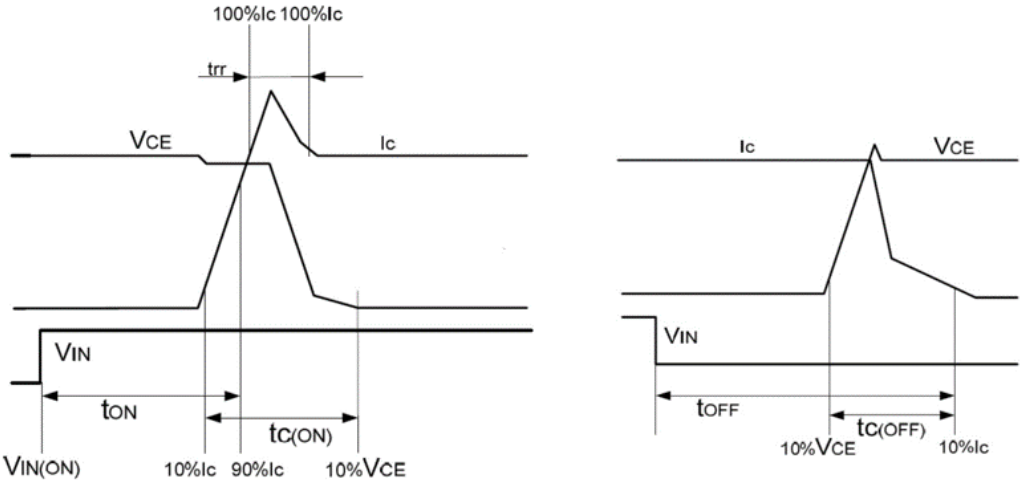
Control Part

Symbol	Parameter	Condition		Min	Typ	Max	Unit
I_{QCC}	Quiescent VCC Supply Current	V_{CC} = 15V V_{IN} = 5V	Applied between VCC and COM	-	-	510	uA
I_{QB}	Quiescent VBS Supply Current	V_{DB} = 15V V_{IN} = 5V	Applied between VB(U) -U,VB(V) - V, VB(W) -W	-	-	210	uA
UV_{CCD}	Low-Side Under-Voltage Protection	VCC Under-Voltage Protection Detection Level		7.4	8.4	9.4	V
UV_{CCR}		VCC Under-Voltage Protection Reset Level		8.0	8.9	9.8	V
UV_{BSD}	High-Side Under-Voltage Protection	VBS Under-Voltage Protection Detection Level		7.4	8.4	9.4	V
UV_{BSR}		VBS Under-Voltage Protection Reset Level		8.0	8.9	9.8	V
V_{TS}	HVIC Temperature Sensing Voltage Output	V_{CC} = 15 V, T_{HVIC} = 25°C （Figure4）		0.6	0.79	0.98	V
V_{IH}	Threshold Voltage	Logic HIGH Level, Applied between VIN and COM		-	-	2.9	V
V_{IL}	OFF Threshold Voltage	Logic Low Level, Applied between VIN and COM		0.8	-	-	V

$V_{F(BSD)}$	BSD Forward voltage	I_F = 0.1 A, TC = 25°C	-	1.35	1.8	V
$t_{rr(BSD)}$	Reverse Recovery Time	I_F = 0.1 A, TC = 25°C	-	80	-	nS

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PN}	Supply Voltage	Applied between P and N	-	300	400	V
V_{CC}	Control Supply Voltage	Applied between VCC and COM	13.5	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between VB and VS	13.5	15.0	16.5	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied between VIN and COM	3.0	-	V_{CC}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	-	0.6	V
t_{dead}	Blanking Time for Preventing Arm-Shor	VCC = VBS = 13.5 ~ 16.5 V, Tj <150°C	1.0	-	-	us
F_{PWM}	PWM Switching Frequency	Tj <150°C	-	15	-	KHz



(a)Turn on (b)Turn off

Fig 3: Switching Time Definition

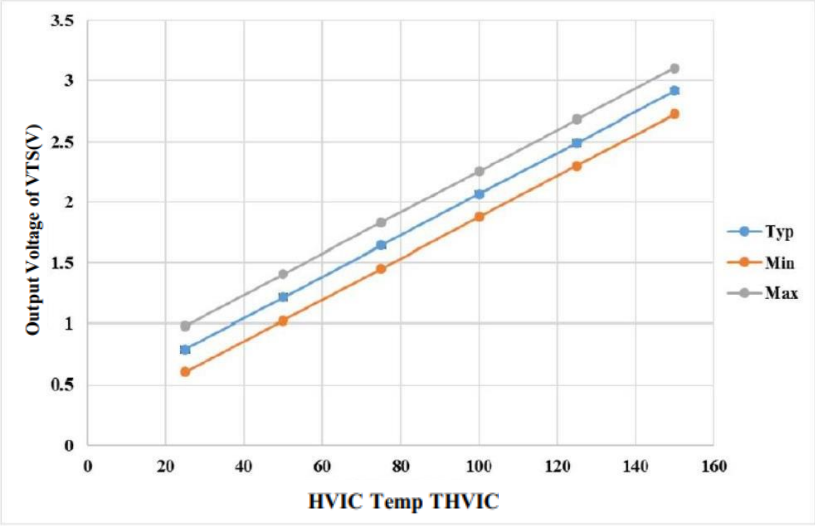


Fig 4: Curves of HVIC Temperature detection—voltage curve

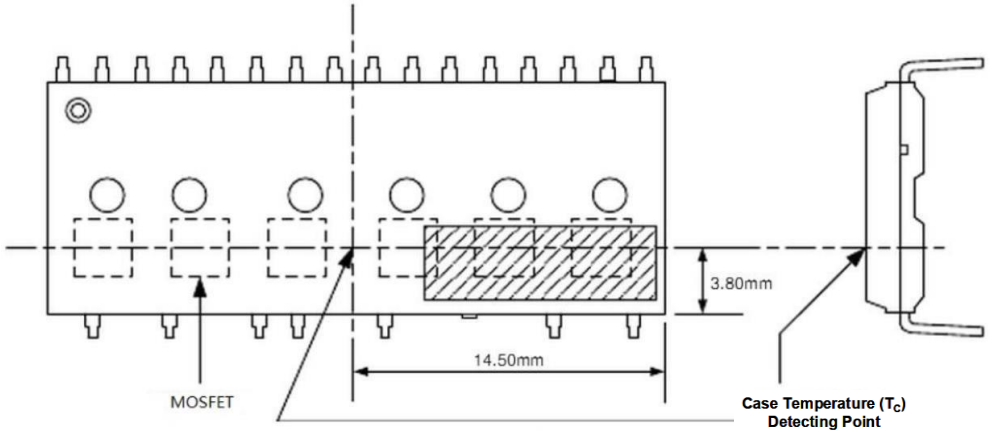


Fig 5：Case Temperature Measurement

Time Charts of Protective Function

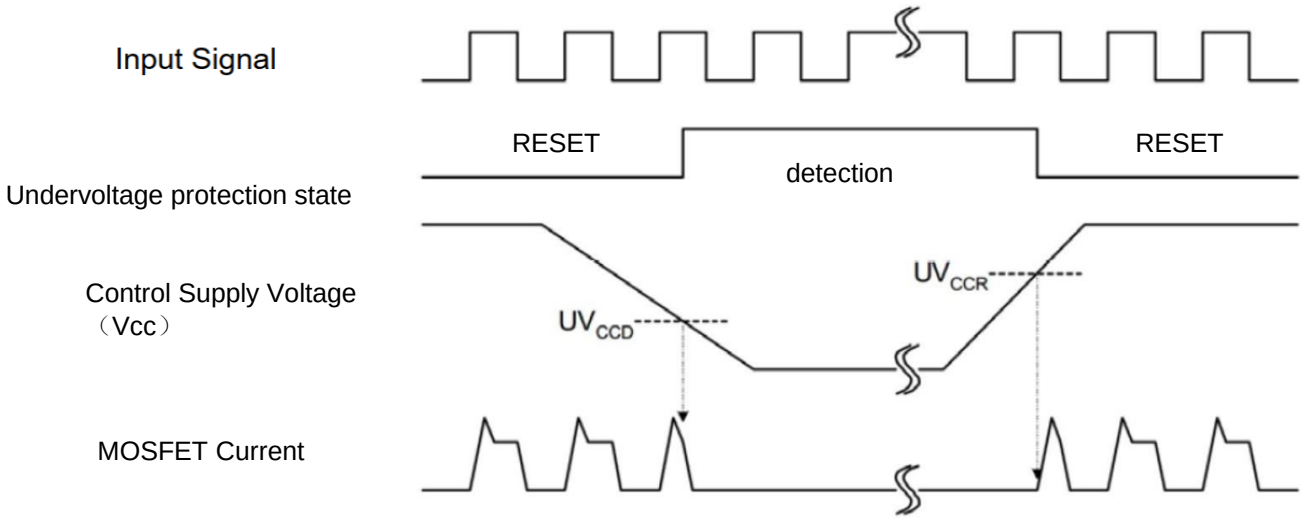


Fig 6：Undervoltage protection sequence diagram (low side)

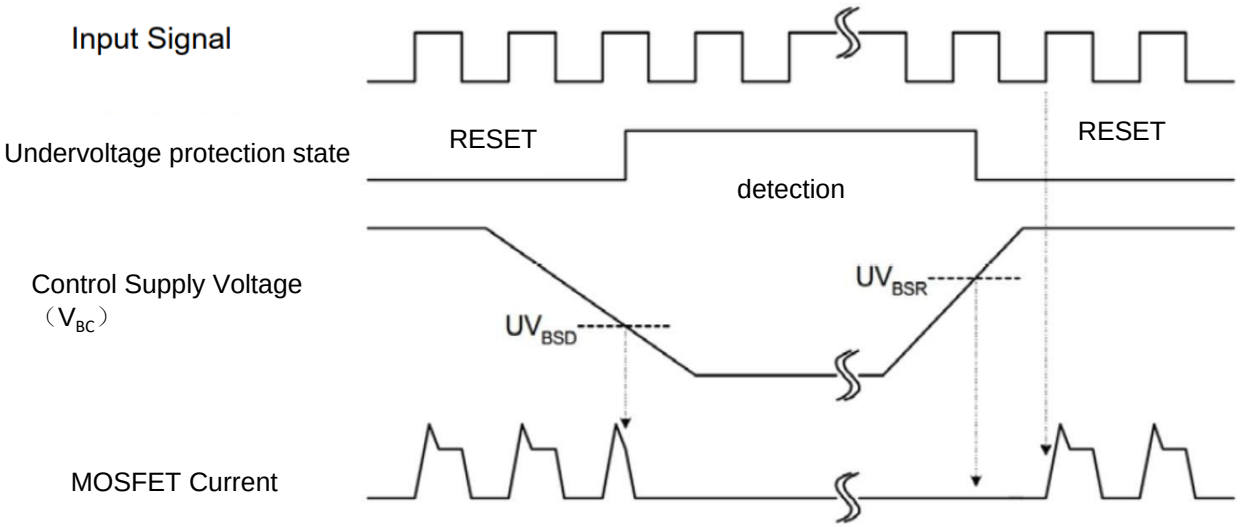
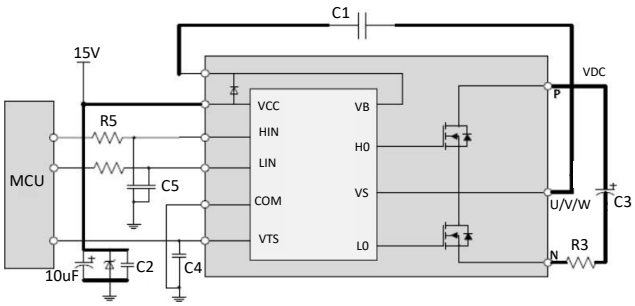


Fig 7：Undervoltage protection sequence diagram (High side)

Application Circuit



HIN	LIN	Output	Note
0	0	High Resistance	Both MOSFET Off
0	1	0	Low side MOSFET On
1	0	VDC	High Side MOSFET On
1	1	Forbidden	Shoot through
Open	Open	High Resistance	Both MOSFET Off

Fig 8：Recommended CPU Interface and Bootstrap Circuit with Parameters

NOTE 4：Parameters for bootsrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is an example of：C1=C2=4.7uF。

NOTE 5：RC coupling(R5 and C5) and C4 at each input of SPM® and MCU may be used to prevent improper signal due to surge noise. Signal input of SPM® is compatible with standard CMOS or LSTTL outputs.

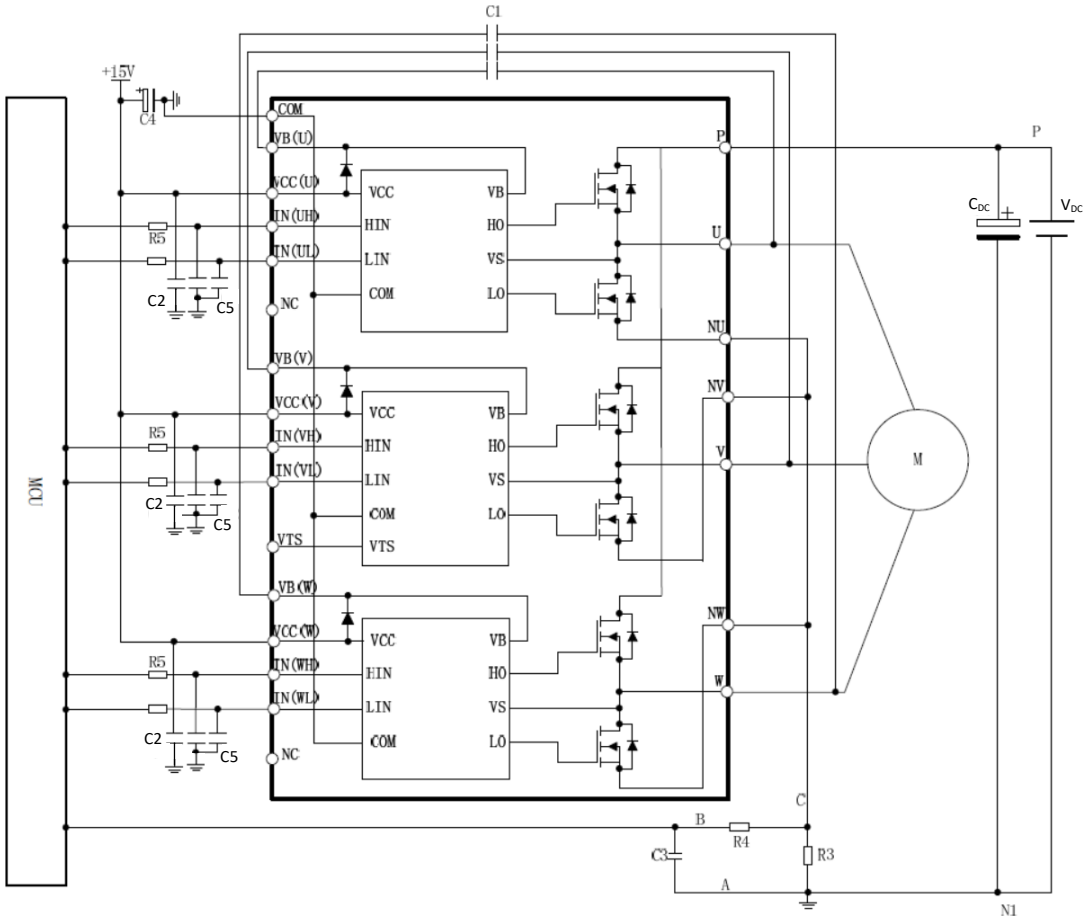


Fig 9：Example of Application Circuit

NOTE 6：，Input drive is High-Active type. There is a 500kΩ(typ.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

NOTE 7：The voltage drop across R3 affects the low side switching performance and the bootstrap characteristics since it is placed between COM and the source terminal of the low side MOSFET. For this reason, the voltage drop across R3 should be less than 1V in the steady-state.

NOTE 8：Thanks for HVIC inside modules, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

NOTE 9：Bootstrap negative electrodes should be connected to U，V，W terminals directly and separated from the main output wires.

NOTE 10：To prevent erroneous protection, the wiring of A, B, C should be as short as possible.

NOTE 11：The time constant R4 、 C3 of the protection circuit should be selected in the range of 1.0-2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R4, C3.

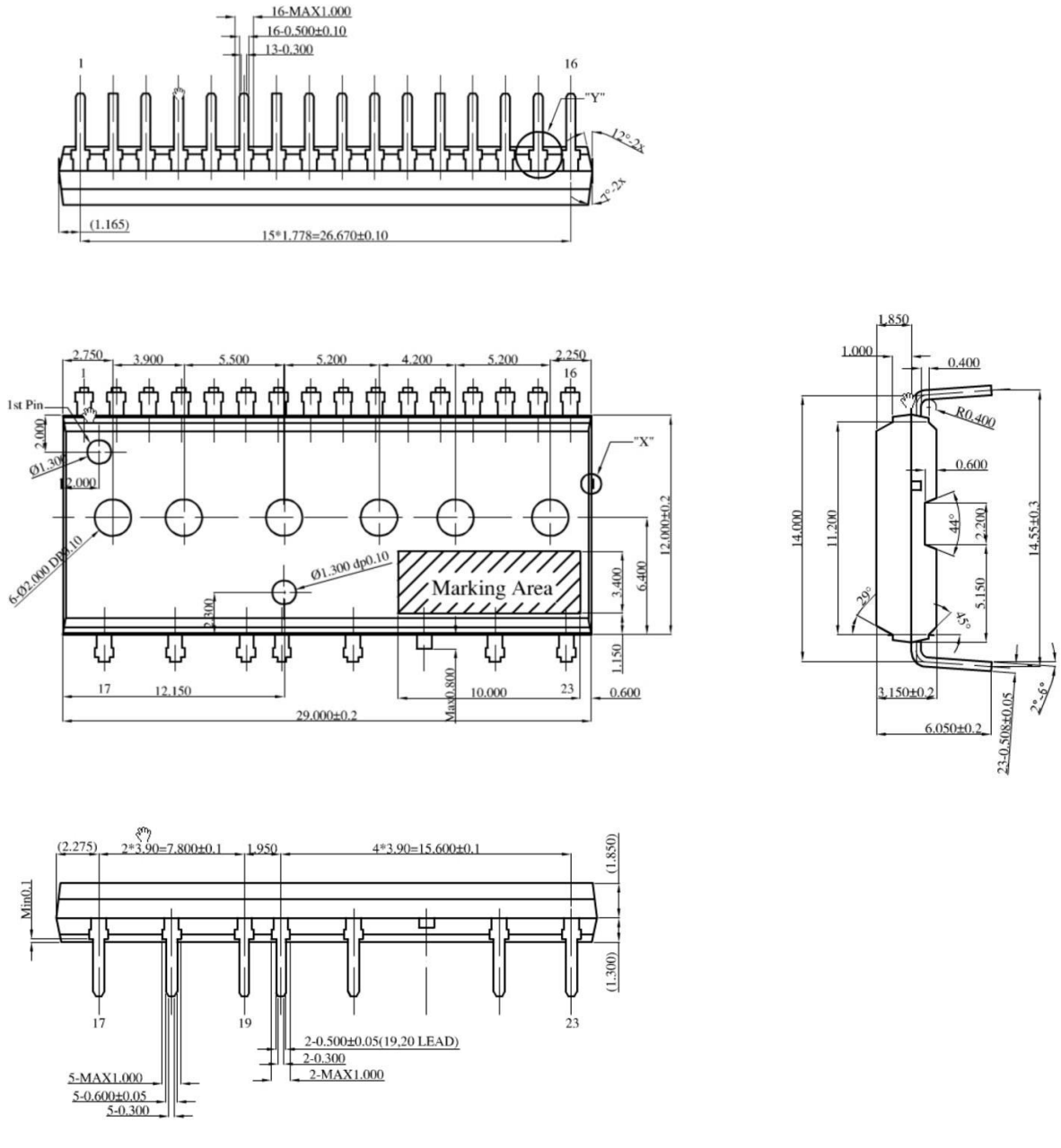
NOTE 12：All capacitors should be mounted as close to the terminals of the IPM as possible.

NOTE 13：To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally, a 0.1-0.22μF snubber between the P-N1 terminals is recommended.

NOTE 14：The terminals of VTS is used to temperature detection, if you don't want to use it, please pull-down the terminal with a 100 KΩ resistor to GND. No connection is forbidden.

Detailed Package Outline Drawings

DIP23-FP



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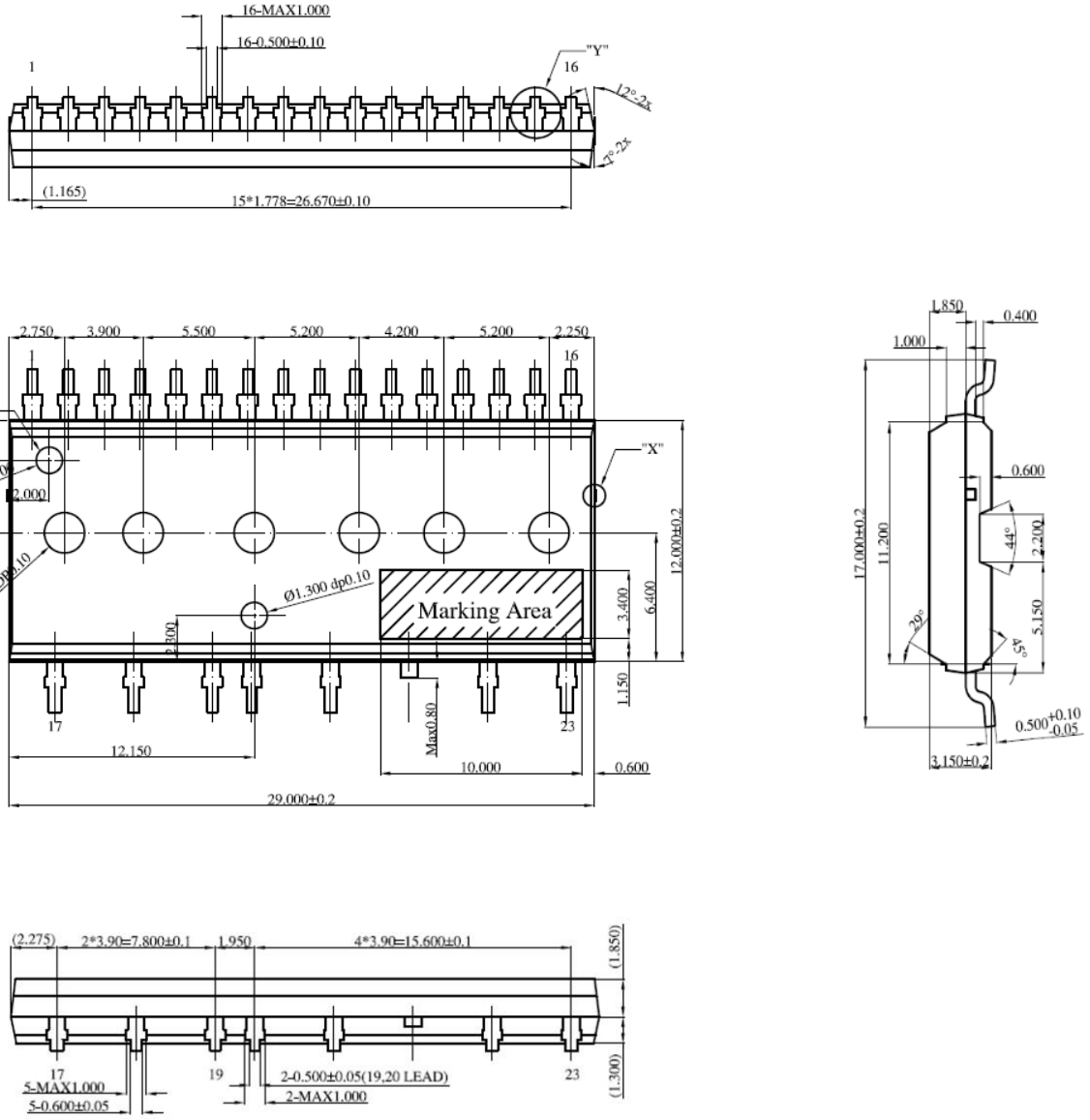
Detailed Package Outline Drawings

SOP23-FP



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